**DSD FISAC-1 Home Assignment (to be submitted on or before 29/10/22)**

**1.**Given the Boolean function F(A,B,C,D) = ∑m(0,3,5,6,8,9,14,15),

1A. Decompose F with respect to A

1B. Decompose F with respect to B

1C. Decompose F with respect to C

1D. Decompose F with respect to D

1E. Find and design the minimal cost implementation of F using 2:1 multiplexer.

1F. Write the Verilog code for the design in 1E.

**2**. For the following functions,

F1 =x’y’z’+xz

F2 = xy’z’+x’y

F3 = x’y’z+xy

2A. Find the canonical SoP of F1,F2 and F3.

2B. Implement F1,F2 and F3 using a decoder and necessary gates.

2C. Write the Verilog code for the decoder implemented in 2B using for loop.

2D. Write the Verilog code for F1,F2 and F3 using the decoder module written in 2C.